PATENT APPLICATION
DOCKET NO.: 1263-0009US

LISTING OF THE CLAIMS

Pursuant to 37 C.F.R. §1.121, provided below is a listing of the pending claims, claims 1-20.

1. (Currently Amended) A compilable semiconductor memory circuit having a plurality of hierarchically organized levels, comprising:

a first level memory portion for storing data therein, said first level memory portion having first level Data In (DIN) and Data Out (DOUT) buffer blocks associated therewith for effectuating data operations with respect to a location in said first level memory portion, said first level DIN buffer block including Local Data In (LDIN) driver circuitry;

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a second level memory portion for storing data therein, said second level memory portion having second level Data In (DIN) and Data Out (DOUT) buffer blocks associated therewith for effectuating data operations with respect to a location in said second level memory portion; and

multiplexing circuitry disposed in said first level DIN buffer block, said multiplexing circuitry being actuatable for providing data accessed through said second level DOUT buffer block

to said LDIN driver circuitry in said first level DIN buffer block, whereby data accessed from said second level memory portion is selectively loaded into said first level memory portion in a ~~substantially simultaneous~~ loading operation that is substantially simultaneous relative to accessing of said data in said second level memory portion.

2. (Original) The compilable semiconductor memory circuit having a plurality of hierarchically organized levels as set forth in claim 1, wherein said first and second level memory portions comprise static random access memory (SRAM).

3. (Original) The compilable semiconductor memory circuit having a plurality of hierarchically organized levels as set forth in claim 1, wherein said first level memory portion comprises SRAM and said second level memory portion comprises dynamic RAM (DRAM).

4. (Currently Amended) The compilable semiconductor memory circuit having a plurality of hierarchically organized levels as set forth in claim 1, further comprising:

a third level memory portion for storing data therein, said third level memory portion having third level Data In (DIN) and Data Out (DOUT) buffer blocks associated therewith for effectuating data operations with respect to a location in said third level memory portion; and

multiplexing circuitry disposed in said second level DIN buffer block, said multiplexing circuitry being actuatable for providing data accessed through said third level DOUT buffer block to LDIN driver circuitry provided in said second level DIN buffer block, whereby data accessed from said third level memory portion is selectively loaded into said second level memory portion in a ~~substantially simultaneous~~ loading operation that is substantially simultaneous relative to accessing of said data in said third level memory portion.

5. (Original) The compilable semiconductor memory circuit having a plurality of hierarchically organized levels as set forth in claim 4, wherein said multiplexing circuitry disposed in said first level DIN buffer block is selectively operable for providing said data accessed through said third level DOUT buffer block to said LDIN driver circuitry in said first level DIN buffer block for substantially simultaneously loading said data into said first level memory portion.

6. (Original) The compilable semiconductor memory circuit having a plurality of hierarchically organized levels as set forth in claim 5, wherein each of said first, second, and third level memory portions is selected from the group consisting of SRAM and DRAM.

7. (Currently Amended) The compilable semiconductor memory circuit having a plurality of hierarchically organized levels as set forth in claim 6, wherein said ~~substantially simultaneous~~ loading operation into said first level memory portion is effectuated using an address calculated by a separate address logic circuit.

8. (Currently Amended) The compilable semiconductor memory circuit having a plurality of hierarchically organized levels as set forth in claim 6, wherein said ~~substantially simultaneous~~ loading operation into said first level memory portion is effectuated using an address that is dependent on an address used for accessing data in one of said second and third level memory portions.

9. (Currently Amended) The compilable semiconductor memory circuit having a plurality of hierarchically organized levels as set forth in claim 6, wherein said ~~substantially simultaneous~~ loading operation into said second level memory portion is effectuated using an address calculated by a separate address logic circuit.

10. (Currently Amended) The compilable semiconductor memory circuit having a plurality of hierarchically organized levels as set forth in claim 6, wherein said ~~substantially simultaneous~~ loading operation into said second level memory portion is effectuated using an address that is dependent on an address used for accessing data in said third level memory portion.

11. (Currently Amended) A memory operation method for use in a compilable semiconductor memory circuit having a plurality of hierarchically organized levels, comprising the steps of:

initiating a data access operation for accessing data in said semiconductor memory circuit;

determining if said data is available in a first level memory portion of said semiconductor memory circuit;

if not, accessing said data in a next level memory portion [[of]] integrated within said semiconductor memory circuit; and

selectively loading said data accessed from said next level memory portion into said first level memory portion in a ~~substantially simultaneous~~ loading operation that is substantially simultaneous relative to said accessing of said data in said next level memory portion.

12. (Original) The memory operation method for use in a compilable semiconductor memory circuit as set forth in claim 11, wherein said next level memory portion is a second level memory portion of said semiconductor memory circuit.

13. (Original) The memory operation method for use in a compilable semiconductor memory circuit as set forth in claim 11, wherein said next level memory portion is a third level memory portion of said semiconductor memory circuit.

14. (Currently Amended) The memory operation method for use in a compilable semiconductor memory circuit as set forth in claim 11, wherein said ~~substantially simultaneous~~ loading operation into said first level memory portion is effectuated using an address calculated by a separate address logic circuit.

15. (Currently Amended) The memory operation method for use in a compilable semiconductor memory circuit as set forth in claim 11, wherein said ~~substantially simultaneous~~ loading operation into said first level memory portion is effectuated using an address that is dependent on an address used for accessing data in said next level memory portion.

16. (Original) The memory operation method for use in a compilable semiconductor memory circuit as set forth in claim 11, wherein said first level memory portion is comprised of static random access memory (SRAM).

17. (Original) The memory operation method for use in a compilable semiconductor memory circuit as set forth in claim 11, wherein said first level memory portion is comprised of dynamic RAM (DRAM).

18. (Original) The memory operation method for use in a compilable semiconductor memory circuit as set forth in claim 11, wherein said next level memory portion is comprised of DRAM.

19. (Original) The memory operation method for use in a compilable semiconductor memory circuit as set forth in claim 11, wherein said next level memory portion is comprised of SRAM.

20. (Original) The memory operation method for use in a compilable semiconductor memory circuit as set forth in claim 11, wherein each of said first and second level memory portions is selected from the group consisting of SRAM and DRAM.